Jaden Rhee

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Education

University of Michigan — Ann Arbor, MI
B.S. Electrical and Electronics Engineering, Minor in Computer Science — Expected 2028

Michigan State University | Honors College — East Lansing, MI
B.S. Electrical Engineering | GPA: 3.7 — Transferred 2026

Experience

ECU Design and Validation Intern, Bosch – Plymouth, MI — April 2026 – Present

- Performed hardware bring-up, system-level validation, and electrical debug of chassis control ECUs across 20+ bench and in-vehicle test scenarios using oscilloscopes, waveform generators, and DMMs
- Isolated I2C, SPI, and UART communication faults and signal integrity issues through targeted waveform analysis and impedance measurements to root-cause failures across ECU subsystems

Systems Engineering Lead, NASA L'SPACE Program – Remote — April 2026 – Present

- Led system-level architecture and trade studies for a simulated NASA mission, defining 15+ subsystem requirements across power, communications, and payload systems
- Coordinated cross-functional design reviews with a 10+ member team to refine mission performance

Research Assistant, Human-Automation Technology Lab, MSU – East Lansing, MI — Sept 2025 – May 2026

- Developed multimodal (audio + inertial) pipelines for real-time speaker and emotion recognition
- Reduced MFCC, RMS, and ZCR feature computation by ~50% for embedded deployment
- Co-authored a multi-variable optimization framework for evaluating edge speaker-verification ML pipelines, accepted to IEEE MWSCAS 2026

Head Manager (Audio and Visual Systems), Korean Presbyterian Church of Metro Detroit — Sept 2019 – June 2025

- Designed and maintained multi-channel audio systems for 500+ person events while leading an 8-member team

Projects

JRWatch (Custom Low-Power BLE Smartwatch, PCB + Zephyr Firmware) — github.com/jadenrhee/JRWatch

- Designed a 36 mm, 4-layer smartwatch PCB in KiCad (nRF52840, nPM1300 PMIC, BMI270 IMU, Sharp memory-in-pixel display) with schematic-as-code (SKiDL) and scripted placement/routing; zero ERC/DRC violations
- Engineered gated power domains with event-driven firmware power states, projecting 15 µA armed-sleep current and 4–8 month battery life on a 150 mAh cell, with every figure itemized against datasheet specs
- Wrote Zephyr RTOS firmware (custom board definition, BLE GATT services, IMU motion-wake interrupts, USB-C DFU) built in GitHub Actions CI; verified USB-C charge path at 2.5× IPC-2221 minimum trace width

WiggleCam (4-Lens Digital Wigglegram Camera, Raspberry Pi 5 + RP2040) — github.com/jadenrhee/wigglecam

- Designed a 76 × 50 mm, 4-layer RP2040 co-processor PCB driving constant-current LED flash with hardware-enforced safety limits, shutter debounce, battery telemetry, and multi-camera sync over I2C/UART
- Built a handheld camera firing four hardware-synchronized 16 MP sensors over one CSI interface (Arducam Camarray), rendering auto-aligned 3D wigglegram GIFs shared to any phone via QR code and Wi-Fi hotspot

Publications

Rhee, J., Kumar, N., Chen, X., et al. *Evaluating Edge Speaker Verification ML Pipelines: A Multi-Variable Optimization Framework*, IEEE MWSCAS 2026 (Accepted)

Skills

Embedded & Hardware: KiCad PCB Design, SKiDL, Oscilloscopes, Logic Analyzers, SWD/JTAG, CANalyzer, Low-Power Design, Signal Integrity, EMC/EMI, DFM/DFT
Protocols & Interfaces: I2C, SPI, UART, CAN, LIN, BLE (GATT), USB, SPMI
Programming: C, C++, Python, MATLAB, Verilog, Java, Zephyr RTOS, Git, GitHub Actions CI
Circuit Design & Power: PMICs, Buck Converters, LDOs, Li-Po Charging, ADCs, DACs, Op-Amps, Power Budgeting
Tools & Libraries: PSpice/LTspice, CST Studio Suite, MATLAB/Simulink, Vivado, OpenCV, NumPy, PyTorch, TensorFlow